

100Gb/s CFP4 Optical Transceiver

RTXM290-701



Features

- *Direct LC receptacle optical interface*
- *Single +3.3V power supply*
- *Hot-pluggable*
- *Operating optical data rate up to 112Gbps*
- *Operating electrical serial data rate up to 28Gbps*
- *10 parallel electrical serial interface*
- *Transmission distance up to 10km*
- *AC coupling of CML signals*
- *1310 nm window cooled EA-DFB LD*
- *PIN ROSA*
- *Low power dissipation(Max:6W)*
- *Built in digital diagnostic function*
- *Operating case temperature range:0℃ to 70℃*
- *Compliant with RoHs*
- *MDIO Communication Interface*

Application

- *OTN-OTU4*
- *Switch to switch interface*
- *Switch to router interface*
- *P to P Access Network*

Standards

- **Compliant with IEEE 802.3ba**
- **Compliant with CFP4 MSA hardware specification, Version 0.1 March 02, 2014**
- **Compliant with CFP MSA management specification, Version 2.2 July 01, 2013**
- **Compliant with ITU-T G.959.1 4I1-9D1F**
- **Compliant with RoHS&WEEE**

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	T _s	°C	-40	+85
Relative Humidity	RH	%	5	85
Power Supply Voltage	V _{cc}	V	-0.5	+3.6
Operating Case Temperature Range	T _c	°C	-5	75
Receiver Damage Threshold Per Lane	P _{dag}	dBm	+5.5	

Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Operating Case Temperature Range	T _c	°C	0		70
Power Supply Voltage	V _{cc}	V	3.2	3.3	3.4
Data rate		Gb/s		103.125	112

Specifications (tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Voltage Supply Electrical Characteristics						
Supply Current	Tx Section Rx Section	I _{cc}	A	-	-	1.8 1
Power Supply Noise		V _{rip}			2% 3%	DC-1MHz 1-10MHz
Dissipation	Class5	P _w	W		6	
Low Power Dissipation		P _{low}	W		2	
Inrush Current	Class5	I _{inrush}	mA/usec		200	
Turn-off Current		I _{turnoff}	mA/usec	-200		
Different Signal Electrical Characteristics						
Single Ended Data Input Swing		mV	55	-	525	
Single Ended Data Output Swing		mV	150	-	500	
Differential Signal Output Resistance		Ω	80		120	
Differential Signal Input Resistance	Signal	Ω	80		120	
3.3V LVCMOS Electrical Characteristics						
Input High Voltage		3.3V _{IH}	V	2.0	-	V _{cc} +0.3
Input Low Voltage		3.3V _{IL}	V	-0.3	-	0.8
Input Leakage Current		3.3I _{IIN}	uA	-10	-	+10
Output High Voltage (I _{OH} =100uA)	High	3.3V _{OH}	V	V _{cc} -0.2	-	-
Output Low Voltage (I _{OL} =100uA)		3.3V _{OL}	V			0.2
Minimum Pulse Width of Control Pin Signal		t _{CNTL}	us	100		
1.2V LVCMOS Electrical Characteristics						

Input High Voltage	1.2VIH	V	0.84	1.5	
Input Low Voltage	1.2VIL	V	-0.3	0.36	
Input Leakage Current	1.2IIN	uA	-100	+100	
Output High Voltage	1.2VOH	V	1.0	1.5	
Output Low Voltage	1.2VOL	V	-0.3	0.2	
Output High Current	1.2IOH	mA		-4	
Output Low Current	1.2IOL	mA	+4		
Input Capacitance	Ci	pF		10	
Optical transmitter Characteristics					
Signaling Rate for Each Lane (100GbE)		Gbps	-	25.78125	
Signaling Rate for Each Lane (OTU4)				27.95249	
Four Lane Wavelength Range	λ_1	nm	1294.53	1295.56	1296.59
	λ_2		1299.02	1300.05	1301.09
	λ_3		1303.54	1304.58	1305.63
	λ_4		1308.09	1309.14	1310.19
Side Mode Suppression Ratio	SMSR	dB	30	-	
Total Average Launch Power	Pt	dBm	-	10.5	
Average Launch Power for Each Lane(100GbE)	Pa	dBm	-4.3	+4.5	2
Average Launch Power for Each Lane(OTU4)			-2.5	+2.9	
Optical Modulation Amplitude for Each Lane	OMA	dBm	-1.3	4.5	3
Transmitter and Dispersion Penalty for Each Lanes(100GbE)	TDP	dB		2.2	
Maximum optical path penalty (OTU4)				1.5	
Average Launch Power of Off Transmitter for Each Lanes	Poff	dBm	-	-30	
Extinction Ratio (100GbE)	EX	dB	4		
Extinction Ratio (OTU4)			7		
RIN ₂₀ OMA		dB/Hz		-130	
Optical Return Loss Tolerance		dB		20	
Transmitter Reflectance		dB		-12	4
Eye Diagram	Compliant with IEEE 802.3ba-LR4/G.959.1 4I1-9D1F				
Optical receiver Characteristics					
Receive Rate for Each Lane(100GbE)		Gbps	-	25.78125	
Receive Rate for Each Lane(OTU4)				27.95249	
Four Lane Wavelength Range	λ_1	nm	1294.53	1295.56	1296.59
	λ_2		1299.02	1300.05	1301.09
	λ_3		1303.54	1304.58	1305.63
	λ_4		1308.09	1309.14	1310.19
Overload Input Optical Power	Pmax	dBm	5.5		5
Average Receive Power for Each Lane(100GbE)	Pin	dBm	-10.6	4.5	6&7
Average Receive Power for Each Lane(OTU4)			-8.8	2.9	
Receive Power In OMA for Each Lane	PinOMA	dBm	-	4.5	
Difference in Receive Power between Any Two Lanes		dBm	-	5.5	
Receiver Sensitivity in OMA for Each Lane(100GbE)	SOMA	dBm		-8.6	8
Receiver Sensitivity in Pa for Each Lane(OTU4)				-10.3	9
Stressed Receiver Sensitivity in				-6.8	10&11

OMA for Each Lane		
Los Assert	dBm	-12
Los De-assert	dBm	-19
Los Hysteresis	dBm	0.2

Note1. The supply current includes CFP module's supply current and test board working current.

Note2. Average launch power ,each lane(min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance

Note3. Even if the TDP<1dB, the OMA(min) must exceed this value

Note4. Transmitter reflectance is defined looking into the transmitter

Note5. The receiver shall be able to tolerate , without damage, continuous exposure to an optical input signal having this average power level

Note6. The average receive power , each lane (max) for 100GBASE-ER4 is larger than the 100BASE-ER4 transmitter value to allow compatibility with 100BASE-LR4 units at short distances

Note7. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance

Note8. Receiver sensitivity (OMA), each lane (max) is informative

Note9. Measured with PRBS $2^{31}-1$ for BER= 10^{-5} . The BER for the OTU4 application is required to be met only after FEC has been applied.

Note10. Measured with conformance test signal at TP3 for BER= 10^{-12}

Note11. conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB;stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

Hardware Control Pins

The CFP Module support real-time control functions via hardware pins, listed in the following table: Hardware Control Pins

Hardware Control Pins							
Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
11	TX_DIS (PRG_CNTL)	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull-Up Note1
14	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull-Up Note1
16	MOD_RSTn	Module Reset(Invert)	I	3.3V LVCMOS	Enable	Reset	Pull-Down Note2

Note1: Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP module

Note2: Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Hardware Alarm Pins							
Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
15	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull-Down Note1
12	RX_LOS (PRG_ALARM)	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

Note1: Pull-Down resistor (<100Ohm) is located within the CFP module. Pull-up should be located on the host

Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in the following table: Management Interface Pins

Management Interface Pins							
Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down

13	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
18	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
17	MDC	MDIO Clock	I	1.2V LVCMOS			
19	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
20	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
21	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Timing Parameters for CFP hardware Signal Pins

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific May depend on current state Condition when signal is applied .See Vendor Datasheet
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time.Please See register"Maximum High-Power-up time"in "CFP MSA Management Interface Specification"
Receiver Loss of Signal Assert Time	t_loss_assert		100	us	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	us	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert	GLB_ALRMn_deassert		150	ms	This is a logical

Delay Time					"OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		20	ms	Value is dependent upon module start-up time.Please See register "Maximum TX-Turn-on Time" in "CFP MSA Management Interface Specification"

High Speed Electrical Characteristics

Reference Clock Characteristics (optional)

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency			161.1328125/644.53125		MHz	1/160or 1/40 of electrical lane rate (100GE)
			174.7031 /698.8123MHz			1/160or 1/40 of electrical lane rate (OTU4)
Frequency Stability	Δf	-100		100	ppm	For Ethernet applications
		-20		20		For Telecom applications
Output Differential Voltage	V _{DIFF}	400		1200	mV	Peak to Peak Differential
RMS jitter ^{1,2}	σ			10	ps	Random Jitter Over frequency band of 10KHz<f<10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10%/90%	t _{r/f}	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

Optional Transmitter and Receiver Monitor Clock Characteristics

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency					MHz	1/8 of Network lane rate
Output Differential Voltage	V _{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

CFP Register Allocation

CFP Register Allocation					
Starting Address in Hex	Ending Address in Hex	Access Type	Allocated Size	Data Bit Width	Table Name and Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 use
8000	807F	RO	128	8	CFP NVR 1. Basic ID register
8080	80FF	RO	128	8	CFP NVR 2. Extended ID register
8100	817F	RO	128	8	CFP NVR 3. Network lane specific registers
8180	81FF	RO	128	8	CFP NVR 4
8200	83FF	RO	4x128	N/A	MSA Reserved
8400	847F	RO	128	8	Vendor NVR 1. Vendor data registers
8480	84FF	RO	128	8	Vendor NVR 2. Vendor data registers
8500	87FF	RO	6x128	N/A	Reserved by CFP MSA
8800	887F	R/W	128	8	User NVR 1. User data registers
8880	88FF	R/W	128	8	User NVR 2. User data registers
8900	8EFF	RO	12x128	N/A	Reserved by CFP MSA
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use
9000	9FFF	RO	4096	N/A	Reserved for vendor private use
A000	A07F	R/W	128	16	CFP Module VR1. CFP Module level control and DDM registers
A080	A0FF	RO	128	16	MLG VR 1. MLG Management Interface registers
A100	A1FF	RO	2x128	N/A	Reserved by CFP MSA
A200	A27F	R/W	128	16	Network Lane VR 1. Network lane specific register
A280	A2FF	R/W	128	16	Network Lane VR 2. Network lane specific register
A300	A3FF	RO	2x128	N/A	Network Lane VR 3. Network Lane n Vendor Specific FAWS Registers.
A400	A47F	R/W	128	16	Host lane VR1. Host lane specific registers
A480	ABFF	RO	15x128	N/A	Reserved by CFP MSA
AC00	AFFF	RW	8x128	16	Common Data Block Registers
B000	BFFF	RW	4096	16	Allocated for OIF MSA-100GLH modules, See Section 6
C000	FFFF	RO	4x4096	N/A	Reserved by CFP MSA

CFP NVR1

CFP NVR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8000	1	RO	7~0	Module Identifier	12	N/A
8001	1	RO	7~0	Extended Identifier	E4	N/A
8002	1	RO	7~0	Connector Type Code	07	N/A
8003	1	RO	7~0	Ethernet Application Code	01	N/A
8004	1	RO	7~0	Fiber Channel Application Code	00	N/A
8005	1	RO	7~0	Copper Link Application Code	00	N/A
8006	1	RO	7~0	SONET/SDH Application Code	00	N/A
8007	1	RO	7~0	OTN Application Code	08	N/A
8008	1	RO	7~0	Additional Capable Rates Supported	18	N/A
8009	1	RO	7~0	Number of Lanes Supported	44	N/A
800A	1	RO	7~0	Media Properties	11	N/A
800B	1	RO	7~0	Maximum Network Lane Bit Rate	8C	0.2Gbps
800C	1	RO	7~0	Maximum host Lane Bit Rate	38	0.2Gbps
800D	1	RO	7~0	Maximum Single Mode Optical Fiber Length	0A	km
800E	1	RO	7~0	Maximum Multi-Mode Mode Optical Fiber Length	00	10m
800F	1	RO	7~0	Maximum Copper Cable length	00	1m
8010	1	RO	7~0	Transmitter Spectral Characteristics1	00	N/A
8011	1	RO	7~0	Transmitter Spectral Characteristics2	04	N/A
8012	2	RO	7~0	Minimum Wavelength per Active Fiber		25pm
8014	2	RO	7~0	Maximum Wavelength per Active Fibe		25pm
8016	2	RO	7~0	Maximum per Lane Optical Width		1pm
8018	1	RO	7~0	Device Technology1		
8019	1	RO	7~0	Device Technology2		
801A	1	RO	7~0	Signal Code		
801B	1	RO	7~0	Maximum Total Optical Output Power per Connector		
801C	1	RO	7~0	Maximum Optical Input Power per Network Lane		
801D	1	RO	7~0	Maximum Power Consumption		
801E	1	RO	7~0	Maximum Power Consumption in Low Power Mode		
801F	1	RO	7~0	Maximum Operating Case Temp Range		
8020	1	RO	7~0	Minimum Operating Case Temp Range		
8021	16	RO	7~0	Vendor Name		
8031	3	RO	7~0	Vendor OUI		
8034	16	RO	7~0	Vendor Part Number		
8044	16	RO	7~0	Vendor Serial Number		
8054	8	RO	7~0	Data Code		
805C	2	RO	7~0	Lot Code		
805E	10	RO	7~0	CLEI Code		
8068	1	RO	7~0	CFP MSA hardware Specification Revision		

				Number		
8069	1	RO	7~0	CFP MSA Management Interface Specification Revision Number		
806A	2	RO	7~0	Module Hardware Version Number		
806C	2	RO	7~0	Module Firmware Version Number		
806E	1	RO	7~0	Digital Diagnostic Monitoring Type		
806F	1	RO	7~0	Digital Diagnostic Monitoring Capability 1		
8070	1	RO	7~0	Digital Diagnostic Monitoring Capability 2		
8071	1	RO	7~0	Module Enhanced Options		
8072	1	RO	7~0	Maximum High-Power-up Time		
8073	1	RO	7~0	Maximum TX-Turn-on Time		
8074	1	RO	7~0	Host Lane Signal Spec		
8075	1	RO	7~0	Heat Sink Type		
8076	1	RO	7~0	Maximum TX-Turn-off Time		
8077	1	RO	7~0	Maximum High-Power-down Time		
8078	1	RO	7~0	Module Enhanced Options 2		
8079	1	RO	7~0	Transmitter Monitor Clock Options		
807A	1	RO	7~0	Receiver Monitor Clock Options		
807B	2	RO	7~0	Module Firmware B VersionNumber		
807D	2	RO	7~0	Maximum MDIO Ready Time		
807E	1	RO	7~0	CFP and CFP2/4 Extended Identifier		
807F	1	RO	7~0	CFP NVR 1 Checksum		

CFP NVR2

Alarm/Warning Threshold Registers

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8080	2	RO	7~0	Transceiver Temp High Alarm Threshold		
8082	2	RO	7~0	Transceiver Temp High Warning Threshold		
8084	2	RO	7~0	Transceiver Temp Low Warning Threshold		
8086	2	RO	7~0	Transceiver Temp Low Alarm Threshold		
8088	2	RO	7~0	VCC High Alarm Threshold		
808A	2	RO	7~0	VCC High Warning Threshold		
808C	2	RO	7~0	VCC Low Warning Threshold		
808E	2	RO	7~0	VCC Low Alarm Threshold		
8090	2	RO	7~0	SOA Bias Current High Alarm Threshold		
8092	2	RO	7~0	SOA Bias Current High Warning Threshold		
8094	2	RO	7~0	SOA Bias Current Low Warning Threshold		
8096	2	RO	7~0	SOA Bias Current Low Alarm Threshold		
8098	2	RO	7~0	Auxiliary 1 Monitor High Alarm Threshold		

809A	2	RO	7~0	Auxiliary 1 Monitor High Warning Threshold		
809C	2	RO	7~0	Auxiliary 1 Monitor Low Warning Threshold		
809E	2	RO	7~0	Auxiliary 1 Monitor Low Alarm Threshold		
80A0	2	RO	7~0	Auxiliary 2 Monitor High Alarm Threshold		
80A2	2	RO	7~0	Auxiliary 2 Monitor High Warning Threshold		
80A4	2	RO	7~0	Auxiliary 2 Monitor Low Warning Threshold		
80A6	2	RO	7~0	Auxiliary 2 Monitor Low Alarm Threshold		
80A8	2	RO	7~0	Laser Bias Current High Alarm Threshold		
80AA	2	RO	7~0	Laser Bias Current High Warning Threshold		
80AC	2	RO	7~0	Laser Bias Current Low Warning Threshold		
80AE	2	RO	7~0	Laser Bias Current Low Alarm Threshold		
80B0	2	RO	7~0	Laser Output Power High Alarm Threshold		
80B2	2	RO	7~0	Laser Output Power High Warning Threshold		
80B4	2	RO	7~0	Laser Output Power Low Warning Threshold		
80B6	2	RO	7~0	Laser Output Power Low Alarm Threshold		
80B8	2	RO	7~0	Laser Temperature High Alarm Threshold		
80BA	2	RO	7~0	Laser Temperature High Warning Threshold		
80BC	2	RO	7~0	Laser Temperature Low Warning Threshold		
80BE	2	RO	7~0	Laser Temperature Low Alarm Threshold		
80C0	2	RO	7~0	Receive Optical Power High Alarm Threshold		
80C2	2	RO	7~0	Receive Optical Power High Warning Threshold		
80C4	2	RO	7~0	Receive Optical Power Low Warning Threshold		
80C6	2	RO	7~0	Receive Optical Power Low Alarm Threshold		
80C8	55	RO	7~0	Reserved		
80FF	1	RO	7~0	CFP NVR 2 Checksum		

CFP NVR3

Network Lane BOL Measurement Registers

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8100	32	RO	7~0	Rx Sensitivity Spec for network lanes 0~15		
8120	32	RO	7~0	Tx Power Spec for network lanes 0~15		
8140	32	RO	7~0	Measured ER for network lanes 0~15		
8160	32	RO	7~0	Path Penalty for network lanes		

				0~15		
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CFP NVR4

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Base ID Information						
8180	1	RO	7~0	CFP NVR3 Checksum		
8181	127	RO	7~1	Reserved		

CFP VR1

Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Module Command/Setup Registers						
A000	2	RO	15~0	Reserved		
A002	2	RO	15~0	Reserved		
A004	1	RO		NVR Access Control		
			8~6	Reserved		
			4	Reserved		
			3~2	Command Status		
		RW	15~9	Reserved		
			5	User Restore and Save Command		
			1~0	Extended Commands		
A005	1	RO		PRG_CNTL3 Function Select		
			15~8	Reserved		
		RW	7~0	Function Select Code		
A006	1	RO		PRG_CNTL2 Function Select		
			15~8	Reserved		
		RW	7~0	Function Select Code		
A007	1	RO		PRG_CNTL1 Function Select		
			15~8	Reserved		
		RW	7~0	Function Select Code		
A008	1	RO		PRG_ALRM3 Source Select		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A009	1	RO		PRG_ALRM2 Source Select		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00A	1	RO		PRG_ALRM1 Source Select		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00B	1	RO		Module Bi-/Uni-Directional Operating Mode Select		
			15~3	Reserved		
		RW	2~0	Module Bi/uni-Direction Mode Select		
A00C	4	RO		Reserved		
Module Control Registers						
A010	1			Module General Control		
		RW/SC/LH	15	Soft Module Reset		
		RW	14	Soft Module Low Power		
		RW	13	Soft TX Disable		
		RW	12	Soft PRG_CNTL3 Control		

		RW	11	Soft PRG_CNTL2 Control		
		RW	10	Soft PRG_CNTL1 Control		
		RW	9	Soft GLB_ALARM Test		
		RO	8~6	Reserved		
		RO	5	TX_DIS Pin State		
		RO	4	MOD_LOPWR Pin State		
		RO	3	PRG_CNTL3 Pin State		
		RO	2	PRG_CNTL2 Pin State		
		RO	1	PRG_CNTL1 Pin State		
		RO	0	Reserved		
A011	1			Network Lane TX Control		
		RO	15	Reserved		
		RW	14	TX PRBS Generator Enable		
		RW	13	TX PRBS Pattern 1		
		RW	12	TX PRBS Pattern 0		
		RW	11	TX De-skew Enable		
		RW	10	TX FIFO Reset		
		RW	9	TX FIFO Auto Reset		
		RW	8	TX Reset		
		RW	7~5	TX MCLK Control		
		RO	4	Reserved		
		RW	3~1	TX Rate Select (10G lane rate)		
		RW	0	TX Reference CLK Rate Select		
				Network Lane RXControl		
A012	1	RW	15	Active Decision Voltageand Phase function		
		RW	14	RX PRBS CheckerEnable		
		RW	13	RX PRBS Pattern 1		
		RW	12	RX PRBS Pattern 0		
		RW	11	RX Lock RX_MCLK to Reference CLK		
		RW	10	Network Lane Loop-back		
		RW	9	RX FIFO Auto Reset		
		RW	8	RX Reset		
		RW	7~5	RX MCLK Control		
		RW	4	RX FIFO Reset		
		RW	3~1	RX Rate Select		
		RW	0	RX Reference CLK Rate Select		
A013	1	RW		Individual Network Lane TX_DIS Control		
			15	Lane 15 Disable		
			14	Lane 14 Disable		
			13	Lane 13 Disable		
			12	Lane 12 Disable		
			11	Lane 11 Disable		
			10	Lane 10 Disable		
			9	Lane 9 Disable		
			8	Lane 8 Disable		
			7	Lane 7 Disable		
			6	Lane 6 Disable		
			5	Lane 5 Disable		
			4	Lane 4 Disable		
			3	Lane 3 Disable		
			2	Lane 2 Disable		
			1	Lane 1 Disable		
			0	Lane 0 Disable		
A014	1			Host Lane Control		
		RO	15	Reserved		

		RW	14	TX PRBS Checker Enable		
		RW	13	TX PRBS Pattern 1		
		RW	12	TX PRBS Pattern 0		
		RO	11	Reserved		
		RW	10	Host Lane Loop-back Enable		
		RO	9	Reserved		
		RO	8	Reserved		
		RW	7	RX PRBS Generator Enable		
		RW	6	RX PRBS Pattern 1		
		RW	5	RX PRBS Pattern 0		
		RO	4~0	Reserved		
A015	1	RO		Reserved		
A016	1	RO		Module State		
			15~9	Reserved		
			8	High-Power-down State		
			7	TX-Turn-off State		
			6	Fault State		
			5	Ready State		
			4	TX-Turn-on State		
			3	TX-Off State		
			2	High-Power-up State		
			1	Low-Power State		
			0	Initialize State		
A017	1	RO		Reserved		
A018	1	RO		Global Alarm Summary		
			15	GLB_ALRM Assertion Status		
			14	Host Lane Fault and Status Summary		
			13	Network Lane Fault and Status Summary		
			12	Network Lane Alarm and Warning Summary		
			11	Module Alarm and Warning 2 Summary		
			10	Module Alarm and Warning 1 Summary		
			9	Module Fault Summary		
			8	Module General Status Summary		
			7	Module State Summary		
			6~1	Reserved		
			0	Soft GLB_ALRM Test Status		
A019	1	RO		Network Lane Alarm and Warning Summary		
			15	Lane 15 Alarm and Warning Summary		
			14	Lane 14 Alarm and Warning Summary		
			13	Lane 13 Alarm and Warning Summary		
			12	Lane 12 Alarm and Warning Summary		
			11	Lane 11 Alarm and Warning Summary		
			10	Lane 10 Alarm and Warning Summary		
			9	Lane 9 Alarm and Warning Summary		
			8	Lane 8 Alarm and Warning Summary		
			7	Lane 7 Alarm and Warning		

				Summary		
			6	Lane 6 Alarm and Warning Summary		
			5	Lane 5 Alarm and Warning Summary		
			4	Lane 4 Alarm and Warning Summary		
			3	Lane 3 Alarm and Warning Summary		
			2	Lane 2 Alarm and Warning Summary		
			1	Lane 1 Alarm and Warning Summary		
			0	Lane 0 Alarm and Warning Summary		
A01A	1	RO		Network Lane Fault and Status Summary		
			15	Lane 15 Fault and Status Summary		
			14	Lane 14 Fault and Status Summary		
			13	Lane 13 Fault and Status Summary		
			12	Lane 12 Fault and Status Summary		
			11	Lane 11 Fault and Status Summary		
			10	Lane 10 Fault and Status Summary		
			9	Lane 9 Fault and Status Summary		
			8	Lane 8 Fault and Status Summary		
			7	Lane 7 Fault and Status Summary		
			6	Lane 6 Fault and Status Summary		
			5	Lane 5 Fault and Status Summary		
			4	Lane 4 Fault and Status Summary		
			3	Lane 3 Fault and Status Summary		
			2	Lane 2 Fault and Status Summary		
			1	Lane 1 Fault and Status Summary		
			0	Lane 0 Fault and Status Summary		
A01B	1	RO		Host Lane Fault and Status Summary		
			15	Lane 15 Fault and Status Summary		
			14	Lane 14 Fault and Status Summary		
			13	Lane 13 Fault and Status Summary		
			12	Lane 12 Fault and Status Summary		
			11	Lane 11 Fault and Status Summary		
			10	Lane 10 Fault and Status Summary		

				Summary		
			9	Lane 9 Fault and Status Summary		
			8	Lane 8 Fault and Status Summary		
			7	Lane 7 Fault and Status Summary		
			6	Lane 6 Fault and Status Summary		
			5	Lane 5 Fault and Status Summary		
			4	Lane 4 Fault and Status Summary		
			3	Lane 3 Fault and Status Summary		
			2	Lane 2 Fault and Status Summary		
			1	Lane 1 Fault and Status Summary		
			0	Lane 0 Fault and Status Summary		
A01C	1	RO		Reserved		
Module FAWS Registers						
A01D	1	RO		Module General Status		
			15	Reserved		
			14	Reserved		
			13	HW_Interlock		
			12~11	Reserved		
			10	Loss of REFCLK Input		
			9	TX_JITTER_PLL_LOL		
			8	TX_CMU_LOL		
			7	TX_LOSF		
			6	TX_HOST_LOL		
			5	RX_LOS		
			4	RX_NETWORK_LOL		
			3	Out of Alignment		
			2	Reserved		
			1	HIPWR_ON		
			0	Reserved		
A01E	1	RO		Module Fault Status		
			15	Reserved		
			14~7	Reserved		
			6	PLD or Flash Initialization Fault		
			5	Power Supply Fault		
			4~2	Reserved		
			1	CFP Checksum Fault		
			0	Reserved		
A01F	1	RO		Module Alarms and Warnings 1		
			15~12	Reserved		
			11	Mod Temp High Alarm		
			10	Mod Temp High Warning		
			9	Mod Temp Low Warning		
			8	Mod Temp Low Alarm		
			7	Mod Vcc High Alarm		
			6	Mod Vcc High Warning		
			5	Mod Vcc Low Warning		
			4	Mod Vcc Low Alarm		
			3	Mod SOA Bias High Alarm		
			2	Mod SOA Bias High Warning		

A020	1	RO	1	Mod SOA Bias Low Warning		
			0	Mod SOA Bias Low Alarm		
				Module Alarms and Warnings 2		
			15~8	Reserved		
			7	Mod Aux 1 High Alarm		
			6	Mod Aux 1 High Warning		
			5	Mod Aux 1 Low Warning		
			4	Mod Aux 1 Low Alarm		
			3	Mod Aux 2 High Alarm		
			2	Mod Aux 2 High Warning		
			1	Mod Aux 2 Low Warning		
			0	Mod Aux 2 Low Alarm		
A021	1	RO		Reserved		
A022	1			Module State Latch		
		RO	15~9	Reserved		
		RO/LH/COR	8	High-Power-down State Latch		
		RO/LH/COR	7	TX-Turn-off State Latch		
		RO/LH/COR	6	Fault State Latch		
		RO/LH/COR	5	Ready State Latch		
		RO/LH/COR	4	TX-Turn-on State Latch		
		RO/LH/COR	3	TX-Off State Latch		
		RO/LH/COR	2	High-Power-up State Latch		
		RO/LH/COR	1	Low-Power State Latch		
		RO/LH/COR	0	Initialize State Latch		
A023	1			Module General Status Latch		
		RO	15	Reserved		
		RO	14	Reserved		
		RO/LH/COR	13	HW_Interlock Latch		
		RO	12~11	Reserved		
		RO/LH/COR	10	Loss of REFCLK Input Latch		
		RO/LH/COR	9	TX_JITTER_PLL_LOL Latch		
		RO/LH/COR	8	TX_CMU_LOL Latch		
		RO/LH/COR	7	TX_LOSF Latch		
		RO/LH/COR	6	TX_HOST_LOL Latch		
		RO/LH/COR	5	RX_LOS Latch		
		RO/LH/COR	4	RX_NETWORK_LOL Latch		
		RO/LH/COR	3	Out of Alignment Latch		
		RO	2~0	Reserved		
A024	1			Module Fault Status latch		
		RO	15~7	Reserved		
		RO/LH/COR	6	PLD or Flash Initialization Fault Latch		
		RO/LH/COR	5	Power Supply Fault Latch		
		RO	4~2	Reserved		
		RO/LH/COR	1	CFP Checksum Fault Latch		
A025	1	RO	0	Reserved		
				Module Alarms and Warnings 1 Latch		
		RO	15~12	Reserved		
		RO/LH/COR	11	Mod Temp High Alarm Latch		
		RO/LH/COR	10	Mod Temp High Warning Latch		
		RO/LH/COR	9	Mod Temp Low Warning Latch		
		RO/LH/COR	8	Mod Temp Low Alarm Latch		
		RO/LH/COR	7	Mod Vcc High Alarm Latch		
		RO/LH/COR	6	Mod Vcc High Warning Latch		
		RO/LH/COR	5	Mod Vcc Low Warning Latch		

		RO/LH/COR	4	Mod Vcc Low Alarm Latch		
		RO/LH/COR	3	Mod SOA Bias High Alarm Latch		
		RO/LH/COR	2	Mod SOA Bias High Warning Latch		
		RO/LH/COR	1	Mod SOA Bias Low Warning Latch		
		RO/LH/COR	0	Mod SOA Bias Low Alarm Latch		
A026	1			Module Alarms and Warnings 2 latch		
		RO	15~8	Reserved		
		RO/LH/COR	7	Mod Aux 1 High Alarm Latch		
		RO/LH/COR	6	Mod Aux 1 High Warning Latch		
		RO/LH/COR	5	Mod Aux 1 Low Warning Latch		
		RO/LH/COR	4	Mod Aux 1 Low Alarm Latch		
		RO/LH/COR	3	Mod Aux 2 High Alarm Latch		
		RO/LH/COR	2	Mod Aux 2 High Warning Latch		
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch		
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch		
A027	1	RO		Reserved		
A028	1			Module Stable Enable		
		RO	15~9	Reserved		
		RW	8	High-Power-down State Enable		
		RW	7	TX-Turn-off State Enable		
		RW	6	Fault State Enable		
		RW	5	Ready State Enable		
		RW	4	TX-Turn-on State Enable		
		RW	3	TX-Off State Enable		
		RW	2	High-Power-up State Enable		
		RW	1	Low-Power State Enable		
		RO	0	Initialize State Enable		
A029	1			Module General Status Enable		
		RW	15	GLB_ALRM Master Enable		
		RO	14	Reserved		
		RW	13	HW Interlock		
		RO	12~11	Reserved		
		RW	10	Loss of REFCLK Input Enable		
		RW	9	TX_JITTER_PLL_LOL Enable		
		RW	8	TX_CMU_LOL Enable		
		RW	7	TX_LOSF Enable		
		RW	6	TX_HOST_LOL Enable		
		RW	5	RX_LOS Enable		
		RW	4	RX_NETWORK_LOL Enable		
		RW	3	Out of Alignment Enable		
		RO	2~0	Reserved		
A02A	1			Module Fault Status Enable		
		RO	15~7	Reserved		
		RW	6	PLD or Flash Initialization Fault Enable		
		RW	5	Power Supply Fault Enable		
		RO	4~2	Reserved		
		RW	1	CFP Checksum Fault Enable		

		RO	0	Reserved		
A02B	1	RO		Module Alarm and Warnings 1 Enable		
			15~12	Reserved		
			11	Mod Temp Hi Alarm Enable		
			10	Mod Temp Hi Warn Enable		
			9	Mod Temp Low Warning Enable		
			8	Mod Temp Low Alarm Enable		
			7	Mod Vcc High Alarm Enable		
			6	Mod Vcc High Warning Enable		
			5	Mod Vcc Low Warning Enable		
			4	Mod Vcc Low Alarm Enable		
			3	Mod SOA Bias High Alarm Enable		
			2	Mod SOA Bias High Warning Enable		
			1	Mod SOA Bias Low Warning Enable		
			0	Mod SOA Bias Low Alarm Enable		
A02C	1			Module Alarms and Warnings Enable		
		RO	15~8	Reserved		
		RW	7	Mod Aux 1 High Alarm Enable		
			6	Mod Aux 1 High Warning Enable		
			5	Mod Aux 1 Low Warning Enable		
			4	Mod Aux 1 Low Alarm Enable		
			3	Mod Aux 2 High Alarm Enable		
			2	Mod Aux 2 High Warning Enable		
			1	Mod Aux 2 Low Warning Enable		
			0	Mod Aux 2 Low Alarm Enable		
A02D	2	RO		Reserved		
Module Analog A/D Value Registers						
A02F	1	RO	15~0	Module Temp Monitor A/D Value		
A030	1	RO	15~0	Module Power supply 3.3 V Monitor A/D Value		
A031	1	RO	15~0	SOA Bias Current A/D Value		
A032	1	RO	15~0	Module Auxiliary 1 Monitor A/D Value		
A033	1	RO	15~0	Module Auxiliary 2 Monitor A/D Value		
A034	4	RO		Reserved		
Module PRBS Registers						
A038	1	RO		Network Lane PRBS Data Bit Count		
			15~10	Exponent		
			9~0	Mantissa		
A039	1	RO		Host Lane PRBS Data Bit Count		
			15~10	Exponent		
			9~0	Mantissa		
A03A	70	RO		Reserved		

CFP Network Lane VR1

Network Lane VR1

Network Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Network Lane FAWS Registers						
A200	16	RO		Network Lane n Alarm and Warning		
			15	Bias High Alarm		
			14	Bias High Warning		
			13	Bias Low Warning		
			12	Bias Low Alarm		
			11	TX Power High Alarm		
			10	TX Power High Warning		
			9	TX Power Low Warning		
			8	TX Power Low Alarm		
			7	Laser Temperature High Alarm		
			6	Laser Temperature High Warning		
			5	Laser Temperature Low Warning		
			4	Laser Temperature Low Alarm		
			3	RX Power High Alarm		
			2	RX Power High Warning		
			1	RX Power Low Warning		
			0	RX Power Low Alarm		
A210	16	RO		Network Lane n Fault and Status		
			15	Lane TEC Fault		
			14	Lane Wavelength Unlocked Fault		
			13	Lane APD Power Supply Fault		
			12~8	Reserved		
			7	Lane TX_LOSF		
			6	Lane TX_LOL		
			5	Reserved		
			4	Lane RX_LOS		
			3	Lane RX_LOL		
			2	Lane RX FIFO error		
			1	Reserved		
			0	Reserved		
Network Lane FAWS Latch Registers						
A220	16	RO/LH/COR		Network Lane n Alarm and Warning Latch		
			15	Bias High Alarm Latch		
			14	Bias High Warning Latch		
			13	Bias Low Warning Latch		
			12	Bias Low Alarm Latch		
			11	TX Power High Alarm Latch		
			10	TX Power High Warning Latch		
			9	TX Power Low Warning Latch		
			8	TX Power Low Alarm Latch		
7	Laser Temperature High					

				Alarm Latch		
			6	Laser Temperature High Warning Latch		
			5	Laser Temperature Low Warning Latch		
			4	Laser Temperature Low Alarm Latch		
			3	RX Power High Alarm Latch		
			2	RX Power High Warning Latch		
			1	RX Power Low Warning Latch		
			0	RX Power Low Alarm Latch		
A230	16	RO/LH/COR		Network Lane n Fault and Status latch		
			15	Lane TEC Fault Latch		
			14	Lane Wavelength Unlocked Fault Latch		
			13	Lane APD Power Supply Fault Latch		
			12~8	Reserved		
			7	Lane TX_LOSF Latch		
			6	Lane TX_LOL Latch		
			5	Reserved		
			4	Lane RX_LOS Latch		
			3	Lane RX_LOL Latch		
			2	Lane RX FIFO Status Latch		
			1~0	Reserved		
A240	16	RO RW		Network Lane n Alarm and Warning Enable		
			15	Bias High Alarm Enable		
			14	Bias High Warning Enable		
			13	Bias Low Warning Enable		
			12	Bias Low Alarm Enable		
			11	TX Power High Alarm Enable		
			10	TX Power High Warning Enable		
			9	TX Power Low Warning Enable		
			8	TX Power Low Alarm Enable		
			7	Laser Temperature High Alarm Enable		
			6	Laser Temperature High Warning Enable		
			5	Laser Temperature Low Warning Enable		
			4	Laser Temperature Low Alarm Enable		
			3	RX Power High Alarm Enable		
			2	RX Power High Warning Enable		
			1	RX Power Low Warning Enable		
			0	RX Power Low Alarm Enable		
A250	16			Network Lane n Fault and Status Enable		
		RW	15	Lane TEC Fault Enable		

		RW	14	Lane Wavelength Unlocked Fault Enable		
		RW	13	Lane APD Power Supply Fault Enable		
		RO	12~8	Reserved		
		RW	7	Lane TX_LOSF Enable		
		RW	6	Lane TX_LOL Enable		
		RO	5	Reserved		
		RW	4	Lane RX_LOS Enable		
		RW	3	Lane RX_LOL Enable		
		RW	2	Lane RX FIFO Status Enable		
		RO	1~0	Reserved		
A260	32	RO		Reserved		

CFP Network Lane VR2

Network Lane VR2						
Network Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Network Lane Control Registers						
A280	16			Network Lane n FEC Controls		
		RW	15~8	Phase Adjustment		
		RW	7~0	Amplitude Adjustment		
A290	16	RO	15~0	Network Lane n PRBS Rx Error Count		
			15~10	Exponent		
			9~0	Mantissa		
Network Lane A/D value Measurement Registers						
A2A0	16	RO	15~0	Network Lane n Laser Bias Current monitor A/D value		
A2B0	16	RO	15~0	Network Lane n Laser Output Power monitor A/D value		
A2C0	16	RO	15~0	Network Lane n Laser Temp Monitor A/D value		
A2D0	16	RO	15~0	Network Lane n Receiver Input Power monitor A/D value		
A2E0	32	RO	15~0	Reserved		

CFP Host lane Lane VR1

Host Lane VR1						
Host Lane VR1						
Hex Addr	Size	Access Type	Bit	Register Name	Content (HEX)	LSB Unit
Host Lane FAWS Status Registers						
A400	16			Host Lane m Fault and Status		
		RO	15~2	Reserved		
		RO	1	Lane TX FIFO Error		
		RO	0	TX_HOST_LOL		
Host Lane FAWS Latch Registers						

A410	16			Host Lane m Fault and Status Latch		
		RO	15~2	Reserved		
		RO/LH/COR	1	Lane TX FIFO Error Latch		
		RO/LH/COR	0	TX_HOST_LOL Latch		
Host Lane FAWS Enable Registers						
A420	16			Host Lane m Fault and Status Enable		
		RO	15~2	Reserved		
		RW	1	Lane TX FIFO Error Enable		
		RW	0	TX_HOST_LOL_Enable		
Host Lane Digital PRBS Register						
A430	16			Host Lane m PRBS TX Error Count		
		RO	15~10	Exponent		
		RW	9~0	Mantissa		
Host Lane Control Registers						
A440	16			Host Lane m Control		
		RO	15~4	Reserved		
		RW	3~0	Signal Pre/De-emphasis		
A450	48	RO		Reserved		

Pin Description

The CFP4 connector has 56 pins which are arranged in Top and Bottom rows. The pin map is shown in Table below. The detailed description of the Bottom row ranges from pin 1 through pin 28 and is shown Table below. The pin orientation is shown below in Figure below.

Figure : CFP4 Pin Map Orientation

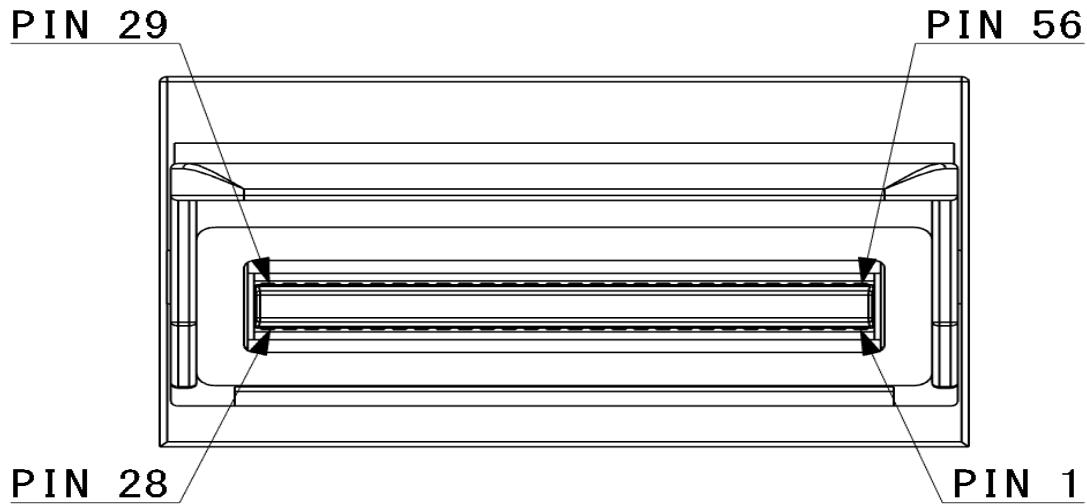


Table : CFP4 Pin-Map

PIN#	Top Row	PIN#	Bottom Row	PIN#	Top Row (ALT1)
56	GND	1	3.3V_GND	56	GND
55	TX3n	2	3.3V_GND	55	TX0n
54	TX3p	3	3.3V	54	TX0p
53	GND	4	3.3V	53	GND

52	TX2n	5	3.3V	52	TX1n
51	TX2p	6	3.3V	51	TX1p
50	GND	7	3.3V_GND	50	GND
49	TX1n	8	3.3V_GND	49	TX2n
48	TX1p	9	VND_IO_A	48	TX2p
47	GND	10	VND_IO_B	47	GND
46	TX0n	11	TX_DIS(PRG_CNTL1)	46	TX3n
45	TX0p	12	RX_LOS(PRG_ALRM1)	45	TX3p
44	GND	13	GLB_ALRMn	44	GND
43	REFCLKn	14	MOD_LOPWR	43	REFCLKn
42	REFCLKp	15	MOD_ABS	42	REFCLKp
41	GND	16	MOD_RSTn	41	GND
40	RX3n	17	MDC	40	RX3n
39	RX3p	18	MDIO	39	RX3p
38	GND	19	PRTADR0	38	GND
37	RX2n	20	PRTADR1	37	RX2n
36	RX2p	21	PRTADR2	36	RX2p
35	GND	22	VND_IO_C	35	GND
34	RX1n	23	VND_IO_D	34	RX1n
33	RX1p	24	VND_IO_E	33	RX1p
32	GND	25	GND	32	GND
31	RX0n	26	MCLKn	31	RX0n
30	RX0p	27	MCLKp	30	RX0p
29	GND	28	GND	29	GND

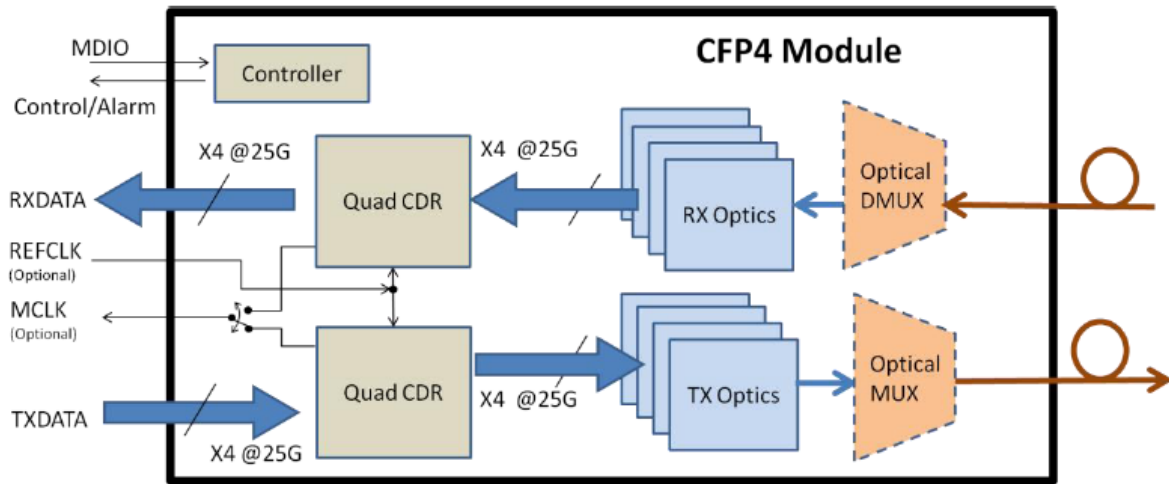
Table: Pin description

PIN#	Name	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separate or tied together with Signal
2	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separate or tied together with Signal
3	3.3V			3.3V Module Supply Votage
4	3.3V			3.3V Module Supply Votage
5	3.3V			3.3V Module Supply Votage
6	3.3V			3.3V Module Supply Votage
7	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separate or tied together with Signal

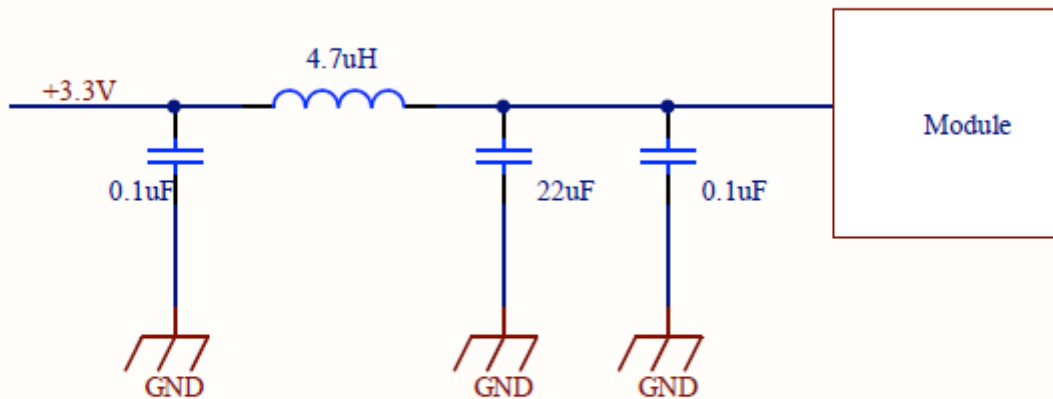
8	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separate or tied together with Signal
9	VND_IO_A	I/O		Module Vendor I/O. Do Not Connect
10	VND_IO_B	I/O		Module Vendor I/O. Do Not Connect
11	TX_DIS(PRG_CNTL1)	I	LVC MOS w/PUR	Transmitter Disable for all lanes, "1" or NC=transmitter disabled,"0"=transmitter enabled (Optionally configurable as Programmable Control1 after Reset)
12	RX_LOS(PRG_ALRM1)	O	LVC MOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset)
13	GLB_ALRMn	O	LVC MOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
14	MOD_LOPWR	I	LVC MOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
15	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
16	MOD_RSTn	I	LVC MOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
17	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
18	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)
19	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
20	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
21	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
22	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect
23	VND_IO_D	I/O		Module Vendor I/O C. Do Not Connect
24	VND_IO_E	I/O		Module Vendor I/O C. Do Not Connect
25	GND	I/O		Module Vendor I/O C. Do Not Connect
26	MCLKn	O	CML	For optical waveform testing. Not for normal use.
27	MCLKp	O	CML	For optical waveform testing. Not for normal use.
28	GND			
29	GND			

30	RX0p	O	CML	Output Data
31	RX0n	O	CML	Inverted Output Data
32	GND			
33	RX1p	O	CML	Output Data
34	RX1n	O	CML	Inverted Output Data
35	GND			
36	RX2p	O	CML	Output Data
37	RX2n	O	CML	Inverted Output Data
38	GND			
39	RX3p	O	CML	Output Data
40	RX3n	O	CML	Inverted Output Data
41	GND			
42	REFCLKp	In	CML	Reference Input Clock
43	REFCLKn	In	CML	Reference Inverted Input Clock
44	GND			
45	TX0p	In	CML	Input Data
46	TX0n	In	CML	Inverted Input Data
47	GND			
48	TX1p	In	CML	Input Data
49	TX1n	In	CML	Inverted Input Data
50	GND			
51	TX2p	In	CML	Input Data
52	TX2n	In	CML	Inverted Input Data
53	GND			
54	TX3p	In	CML	Input Data
55	TX3n	In	CML	Inverted Input Data
56	GND			

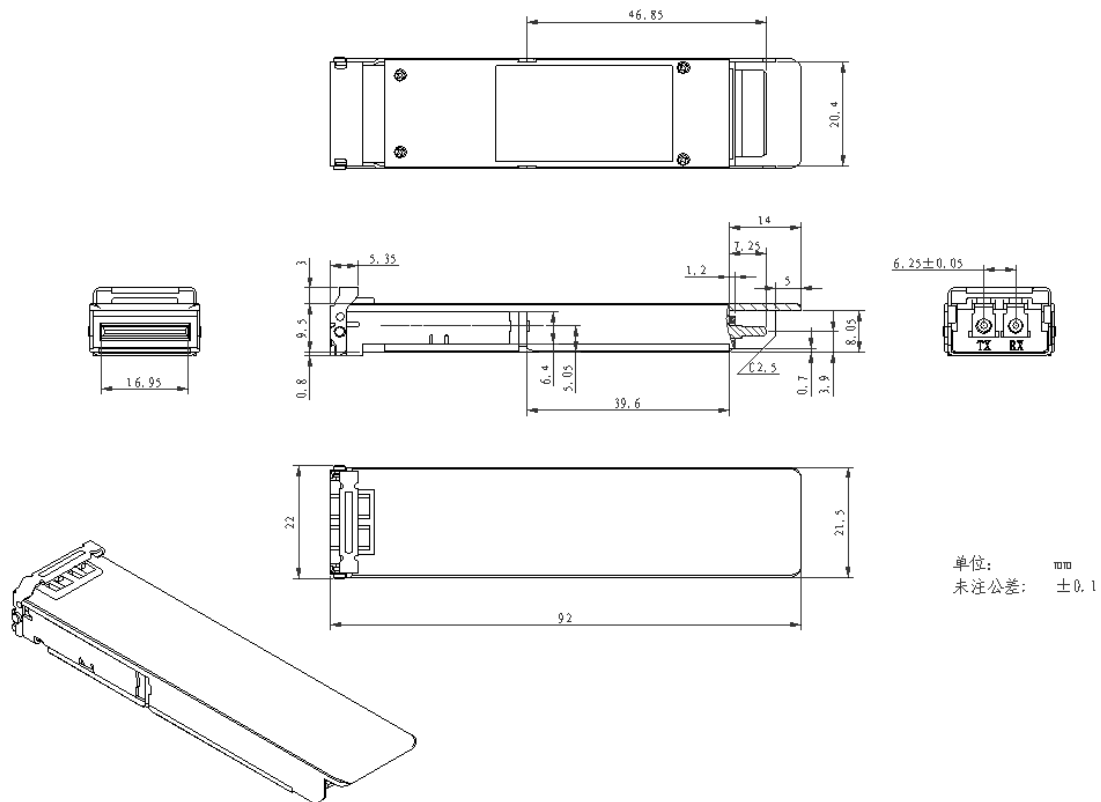
Block diagram



Required Host Board Components



Package outline



Regulatory Compliance

Feature	Test Method		Performance
Electrostatic Discharge (ESD) to the Electrical Pins	Discharge	MIL-STD-883E Method 3015.7	high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B
			the other pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B
Electrostatic Discharge (ESD) Immunity	Discharge	IEC61000-4-2 Class B	15kV air discharges during operation and 8kV direct contact discharge
Electromagnetic Interference (EMI)	CISPR22 ITE Class B		Compliant with standard
	FCC Class B CENELEC EN55022 VCCI Class 1		
Immunity		IEC61000-4-3 Class 2	Compliant with any electro-magnetic regulations
Safety	FDA		

	CDRH 21-CFR 1040 Class 1
	UL
	TUV-GS
	CE

Ordering Information

Part No	Specifications									Application
	Pack	Data rate	Tx	Pout	Rx	S	Top	Reach	Others	Code
RTXM290-701 CFP4		103.125/111.8 Gbps	1310nm	-2.5~+2.9 dBm	PIN <-8.6dBm	0~70℃	10km	DDM	100GbE/OTU4	
			LAN							
			Cooled							
			EMA							
			DFB-LD							